UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/649,050	08/27/2003	Chun Chen	2008.006000/00-0879	4950

23720 7590 12/07/2005

WILLIAMS, MORGAN & AMERSON, P.C.
10333 RICHMOND, SUITE 1100
HOUSTON, TX 77042

EXAMINER	
LUU, CHUONG A	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 12/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H·D

Office Action Summary	Application No.	Applicant(s)	
	10/649,050	CHEN ET AL.	
	Examiner	Art Unit	
	Chuong A. Luu	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 03 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 26 September 2005.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-29 is/are pending in the application.

4a) Of the above claim(s) 29 is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-28 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Double Patenting

Statutory Basis

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Furthermore, there is no apparent reason why applicant would be prevented from presenting claims corresponding to those of the instant application in the other copending application. See *In re Schneller*, 397 F.2d 350, 158 USPQ 210 (CCPA 1968). See also MPEP § 804.

Claims 1-28 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1 and 10 of Chen et al. (U.S. Patent No. 6,737,320 B2) in view of Arai (U.S. 6,111,287). Chen teaches the basic features of applicant's claims but does not specifically claim the use of polysilicon as the material of the floating gates. However, Arai discloses a semiconductor device with using the polysilicon material for the floating gates (see column 2, lines 10-14). Therefore, it would have been obvious to one of ordinary skill in the art to modify the teaching of Nishioka (accordance with the teaching of Van Buskirk) by selecting tungsten as an interconnect material since it has been held to be within the general skill

of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice, In re Leshin, 125 USPQ 416. Doing so would facilitate the manufacture of the semiconductor device and improve the speed of the semiconductor structure. For these reasons, claims 1-28 are seen as obvious variations of the patented claims.

PRIOR ART REJECTIONS

Statutory Basis

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

The Rejections

Claims 1-10, 13, 15-16, 18, 20, 22, 24-25 and 27 are rejected under 35 U.S.C. 102(b) as being anticipated by Lim et al. (U.S. 5,841.161).

Lim discloses a flash memory with

(1) forming a first dielectric layer (22) on a semiconductor substrate (21);

forming a floating gate (23, 25, 27) above the first dielectric layer (22), the floating gate comprised of a first layer doped with a first type of dopant material (see column 3, lines 49-50) and a second layer doped with a second type of dopant material

(see column 3, lines 63-64) that is opposite the first type of dopant material in the first layer;

forming a second dielectric layer (28) above the floating gate (23, 25, 27);

forming a control gate (29) above the second dielectric layer (28) (see Figure 4E);

forming a source (30) and a drain (31) in the substrate (21) (see Figure 4F);

(2) wherein forming the first layer of said floating gate comprises forming a first polysilicon layer above the dielectric layer (see Figure 4A);

(3) wherein forming the first layer of said floating gate comprises depositing the first polysilicon layer and introducing dopant atoms of the first type of dopant into the first polysilicon layer during the deposition process (see column 3, lines 49-50);

(4) wherein forming the first polysilicon layer comprises performing an ion implantation process to introduce dopant atoms of the first type of dopant material into the first polysilicon layer (see column 3, lines 49-50);

(5) wherein forming the floating gate comprises forming a second polysilicon layer above the first polysilicon layer.;

(6) wherein forming the second polysilicon layer comprises depositing the second polysilicon layer and introducing dopant atoms of the second type of dopant material into the second polysilicon layer during the deposition process;

(7) wherein forming the second polysilicon layer comprises performing an ion implantation process to introduce dopant atoms of the second type of dopant material into the second polysilicon layer;

(8) wherein forming the floating gate further comprises forming a barrier layer between the first polysilicon layer and the second polysilicon layer;

(9) wherein forming the first polysilicon layer above the dielectric layer and forming the second polysilicon layer above the first polysilicon layer comprises depositing the first polysilicon layer above the dielectric layer and depositing the second polysilicon layer above the first polysilicon layer;

(10) wherein forming the first polysilicon layer above the dielectric layer and the second polysilicon layer above the first polysilicon layer further comprises performing a first ion implantation process at a first energy to introduce dopant atoms of the first type of dopant materîal into the first polysilicon layer and performing a second ion implantation process at a second energy to introduce dopant atoms of the second type of dopant material into the second polysilicon layer with a second dopant, wherein the first energy is larger than the second energy;

(13) wherein forming the floating gate further comprises forming a barrier layer between the first polysilicon layer and the second polysilicon layer;

(15) forming a first dielectric layer on a semiconductor substrate;

forming a first polysilicon layer above the first dielectric layer;

forming a banier layer above the first polysilicon layer;

forming a second polysilicon layer above the barrier layer;

forming a second dielectric layer above the second polysilicon layer;

forming a control gate above the second (lielectric layer; and

forming a source and a drain in the substrate;

(16) wherein forming the first polysilicon layer comprises depositing the first polysilicon layer and introducing dopant atoms of the first type of dopant material into the first polysilicon layer during the deposition process;

(18) wherein forming the first polysilicon layer comprises performing an ion implantation process to introduce dopant atoms of the first type of dopant material into the first polysilicon layer;

(20) wherein forming the second polysilicon layer comprises depositing the second polysilicon layer and introducing dopant atoms of the second type of dopant material into the secend polysilicon layer during the deposition process;

(22) wherein forming the second polysilicon layer comprises performing an ion implantation process to introduce dopant atoms of the second type of dopant material into the second polysilicon layer;

(24) forming a first dielectric layer on a semiconductor substrate;

forming a first polysilicon layer above the first dielectric layer;

forming a banier layer above the first polysilicon layer;

forming a second polysilicon layer above the barrier layer;

forming a second dielectric layer above the second polysilicon layer; forming a control gate above the second dielectric layer; forming a source and a drain in the substrate;

(25) wherein performing the first ion implantation process comprises performing the first ion implantation process at the first energy such that an ion implant range is at about a mid-point of the first polysilicon layer;

(27) wherein performing the second ion implantation process comprises performing the second ion implantation process at the second energy such that an ion implant range is at about a mid-point of the second polysilicon layer.

PRIOR ART REJECTIONS

Statutory Basis

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The Rejections

Claims 11-12, 14, 17, 19, 21, 23, 26 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lim et al. (U.S. 5,841.161).

Lim teaches the above outlined features except for the dopant doses and the thickness of the barrier layer. However, the dopant doses and the thickness of the barrier layer are considered obvious. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the teaching of Lim by selecting the dopant doses and the thickness of the barrier layer since it has been held that where the general conditions of a claim are disclosed in the prior ad, discovering the optimum or workable ranges involves only routine skill in the art and it is

noted that the applicant does not disclose criticality in the ranges claimed. In re Aller, 105 USPQ 233 (see MPEP 2144.05). Doing so would facilitate the manufacture of the semiconductor device and improve the speed of the semiconductor structure.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chuong A. Luu whose telephone number is (571) 272-1902. The examiner can normally be reached on M-F (6:15-2:45).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David C. Nelms can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chuong Anh Luu
Paten Examiner
December 2, 2005